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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Priority Application Serial No. 09/332,271
Priority Filing Date ..... June 11, 1999
Inventor ..... Klaus Florian Schuegraf et al.
Assignee ..... Micron Technology, Inc.
Priority Group Art Unit 2815
Priority Examiner ..... E. Lee
Attorney's Docket No. MI22-1741
Title: Methods for Forming Wordlines, Transistor Gates, and Conductive Interconnects, and Wordline, Transistor Gate, and Conductive Interconnect Structures

jc996 U.S. PTO 09/875501 06/04/01

INFORMATION DISCLOSURE STATEMENT

References -- See Attached Form PTO-1449

The attached form PTO-1449 is submitted in compliance with 37 CFR §1.56. No admission is made regarding whether the submitted references are prior art.

The listed references were cited by, or submitted to, the Office in the parent, co-pending application of the above-identified application. The above-identified application is a divisional of co-pending Application Serial No. 09/332,271, filed on June 11, 1999. Such prior disclosure is sufficient for the above-identified application as far as copies of the references are concerned.

Citation of these references is respectfully requested.

Respectfully submitted,

Dated: 6-4-01

Attorney: _____
D. Brent Kenady
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